

**I. AMENDMENTS TO THE CLAIMS**  
**(COMPLETE LISTINGS OF ALL CLAIMS)**

1. (currently amended): A nonvolatile memory device, comprising:  
a substrate of a semiconductor material having a first conductivity type;  
a semiconductor block over said substrate and having a first sidewall and a second sidewall opposite to each other and a top between said first sidewall and said second sidewall, said semiconductor block including a first region having a second conductivity type, a second region having said second conductivity type, and a third region between said first region and said second region and having said first conductivity type;  
an electrically conductive folded floating gate over said third region of said semiconductor block, said folded floating gate having a first section adjacent said first sidewall of said semiconductor block, a second section adjacent said second sidewall of said semiconductor block, and a third section adjacent said top of said semiconductor block; and  
a control gate disposed over said third section of said folded floating gate.
2. (original): The nonvolatile memory device of claim 1, said semiconductor block having a height between approximately 0.1 micrometer ( $\mu\text{m}$ ) and approximately 1  $\mu\text{m}$  and a width between approximately 0.05  $\mu\text{m}$  and approximately 0.8  $\mu\text{m}$ .
3. (original): The nonvolatile memory device of claim 1, said semiconductor block having a height and a width, said height being greater than said width.
4. (original): The nonvolatile memory device of claim 1, said semiconductor block having a trapezoidal cross section.
5. (original): The nonvolatile memory device of claim 1, further comprising an insulating layer between said semiconductor block and said substrate.
6. (original): The nonvolatile memory device of claim 1, said control gate including:

a polycrystalline silicon layer adjacent said third section of said folded floating gate;  
and  
a metalized polycrystalline silicon layer over said polycrystalline silicon layer.

7. (original): The nonvolatile memory device of claim 1, further comprising:  
a dielectric layer over said control gate; and  
a tunneling gate over said dielectric layer.
8. (original): The nonvolatile memory device of claim 1, said semiconductor block further including a fourth region having said second conductivity type adjacent said second region, a fifth region of said second conductivity type, and a sixth region of said first conductivity type between said fourth region and said fifth region.
9. (currently amended): The nonvolatile memory device of claim 8, further comprising a second electrically conductive folded floating gate over said sixth region of said semiconductor block, said second folded floating gate having a first section adjacent said first sidewall of said semiconductor block, a second section adjacent said second sidewall of said semiconductor block, and a third section adjacent said top of said semiconductor block.
10. (original): The nonvolatile memory device of claim 9, said control gate being further disposed over said third section of said second folded floating gate.
11. (original): The nonvolatile memory device of claim 10, further comprising:  
a dielectric layer over said control gate;  
a first tunneling gate over said dielectric layer and overlying said folded floating gate;  
and  
a second tunneling gate over said dielectric layer and overlying said second folded floating gate.
12. (currently amended): The nonvolatile memory device of claim 10, further comprising:

a second semiconductor block over said substrate and having a first sidewall and a second sidewall opposite to each other and a top between said first sidewall and said second sidewall, said second semiconductor block including:

- a first region having said second conductivity type, a second region having said second conductivity type, and a third region between said first region and said second region and having said first conductivity type; and
- a fourth region having said second conductivity type adjacent said second region, a fifth region of said second conductivity type, and a sixth region of said first conductivity type between said fourth region and said fifth region;

a third electrically conductive folded floating gate over said third region of said second semiconductor block, said third folded floating gate having a first section adjacent said first sidewall of said second semiconductor block, a second section adjacent said second sidewall of said second semiconductor block, and a third section adjacent said top of said second semiconductor block;

a fourth electrically conductive folded floating gate over said sixth region of said second semiconductor block, said fourth folded floating gate having a first section adjacent said first sidewall of said second semiconductor block, a second section adjacent said second sidewall of said second semiconductor block, and a third section adjacent said top of said second semiconductor block; and

a second control gate disposed over said third section of said third folded floating gate and said third section of said fourth folded floating gate.

13. (original): The nonvolatile memory device of claim 12, further comprising:
  - a dielectric layer over said control gate and said second control gate;
  - a first tunneling gate over said dielectric layer overlying said folded floating gate and said third folded floating gate; and
  - a second tunneling gate over said dielectric layer overlying said second folded floating gate and said fourth folded floating gate.

14. (original): The nonvolatile memory device of claim 12, further comprising an insulating layer insulating said semiconductor block and said second semiconductor block from said substrate.
15. (currently amended): The nonvolatile memory device of claim 1, further comprising:  
a second semiconductor block over said substrate and having a first sidewall and a second sidewall opposite to each other and a top between said first sidewall and said second sidewall, said second semiconductor block including a first region having said second conductivity type, a second region having said second conductivity type, and a third region between said first region and said second region and having said first conductivity type;  
a second electrically conductive folded floating gate over said third region of said second semiconductor block, said second folded floating gate having a first section adjacent said first sidewall of said second semiconductor block, a second section adjacent said second sidewall of said second semiconductor block, and a third section adjacent said top of said second semiconductor block.
16. (original): The nonvolatile memory device of claim 15, further comprising an insulating layer insulating said semiconductor block and said second semiconductor block from said substrate.
17. (original): The nonvolatile memory device of claim 15, said control gate being further disposed over said third section of said second folded floating gate.
18. (original): The nonvolatile memory device of claim 17, further comprising:  
a dielectric layer over said control gate;  
a first tunneling gate over said dielectric layer overlying said folded floating gate; and  
a second tunneling gate over said dielectric layer overlying said second folded floating gate.
19. (original): The nonvolatile memory device of claim 15, further comprising a second control gate disposed over said third section of said second folded floating gate.

20. (original): The nonvolatile memory device of claim 19, further comprising:  
a dielectric layer over said control gate and said second control gate; and  
a tunneling gate over said dielectric layer overlying said folded floating gate and said second folded floating gate.
21. (currently amended): A nonvolatile memory device, comprising:  
a semiconductor substrate of a first conductivity type;  
a plurality of semiconductor blocks over said substrate, each having a first sidewall and a second sidewall, and a top between said first sidewall and said second sidewall, each of said plurality of semiconductor blocks further including a first region of a second conductivity type, a second region of said second conductivity type, and a third region between said first region and said second region and of said first conductivity type;  
a plurality of electrically conductive folded floating gates, each over said third region of a corresponding one of said plurality of semiconductor blocks and having a first section, a second section, and a third section adjacent said first sidewall, said second sidewall, and said top, respectively, of said corresponding semiconductor block; and  
a plurality of control gates disposed over said plurality of folded floating gates.
22. (original): The nonvolatile memory device of claim 21, wherein each of said semiconductor blocks has a height between approximately 0.1 micrometer ( $\mu\text{m}$ ) and approximately 1  $\mu\text{m}$  and a width between approximately 0.05  $\mu\text{m}$  and approximately 0.8  $\mu\text{m}$ .
23. (original): The nonvolatile memory device of claim 21, wherein each of said semiconductor blocks has a trapezoidal cross section.
24. (original): The nonvolatile memory device of claim 21, further comprising an insulating layer between said plurality of semiconductor blocks and said substrate.

25. (original): The nonvolatile memory device of claim 21, further comprising a tunneling gate over said plurality of control gates.
26. (original): The nonvolatile memory device of claim 21, wherein each of said plurality of semiconductor blocks further includes a fourth region having said second conductivity type adjacent said second region, a fifth region of said second conductivity type, and a sixth region of said first conductivity type between said fourth region and said fifth region.
27. (currently amended): The nonvolatile memory device of claim 26, further comprising a second plurality of electrically conductive folded floating gates, each over said sixth region of said corresponding semiconductor block and having a first section, a second section, and a third section adjacent said first sidewall, said second sidewall, and said top respectively, of said corresponding semiconductor block.
28. (original): The nonvolatile memory device of claim 27, wherein said plurality of control gates are further disposed over said third section of said second plurality of folded floating gates.
29. (original): The nonvolatile memory device of claim 28, further comprising:  
a first tunneling gate over said plurality of folded floating gates; and  
a second tunneling gate over said second plurality of folded floating gates.
30. (currently amended): The nonvolatile memory device of claim 21, further comprising:  
a second plurality of semiconductor blocks over said substrate, each including a first region of said second conductivity type, a second region of said second conductivity type, and a third region between said first region and said second region and of said first conductivity type;  
a second plurality of electrically conductive folded floating gates, each over said third region of a corresponding one of said second plurality of semiconductor blocks;  
and

wherein said plurality of control gates are further disposed over said second plurality of folded floating gates.

31. (currently amended): A nonvolatile memory array, comprising:
  - a semiconductor substrate;
  - a plurality of semiconductor stripes over said substrate substantially parallel to one another, each having a first sidewall and a second sidewall, and a top between said first sidewall and said second sidewall, each of said plurality of stripes further including a plurality of sequentially arranged cells, each cell including a source region, a drain region, and a channel region there between;
  - a plurality of electrically conductive folded floating gates arranged in a plurality of rows and a plurality of columns, each over said channel region in a corresponding cell and having a first section, a second section, and a third section adjacent said first sidewall, said second sidewall, and said top, respectively, of a corresponding stripe; and
  - a plurality of control gates, each disposed over a row of said plurality of folded floating gates.
32. (original): The nonvolatile memory array of claim 31, wherein each of said stripes has a height between approximately 0.1 micrometer ( $\mu\text{m}$ ) and approximately 1  $\mu\text{m}$  and a width between approximately 0.05  $\mu\text{m}$  and approximately 0.8  $\mu\text{m}$ .
33. The nonvolatile memory array of claim 31, wherein each of said stripes has a trapezoidal cross section.
34. (original): The nonvolatile memory array of claim 31, further comprising an insulating layer between said plurality of stripes and said substrate.
35. (original): The nonvolatile memory array of claim 31, further comprising a plurality of tunneling gates over said plurality of control gates, each overlying a column of said plurality of folded floating gates.